ABSTRACT OF THE DISCLOSURE

An integrated circuit device having a selectable data rate clock data recovery (CDR) circuit and a selectable data rate transmit circuit. The CDR circuit includes a receive circuit to capture a plurality of samples of an input signal during a cycle of a first clock signal. A select circuit is coupled to the receive circuit to select, according to a receive data rate select signal, one of the plurality of samples to be a first selected sample of the input signal and another of the plurality of samples to be a second selected sample of the input signal. A phase control circuit is coupled to receive the first and second selected samples of the input signal and includes circuitry to compare the selected samples to determine whether the first clock signal leads or lags a transition of the input signal. The transmit circuit includes a serializing circuit to receive a parallel set of bits and to output the set of bits in sequence to an output driver in response to a first clock signal. A select circuit selects, according to a transmit data rate select signal, data bits within an outbound data value to form the parallel set of bits received within the serializing circuit. Bits within the outbound data value are selected to achieve a first data rate when the transmit data rate select signal is in a first state, and to achieve a second data rate when the transmit data rate select signal is in a second state.